



Laxmi Singh Charitable Trust's (Regd.)

THAKUR COLLEGE OF ENGINEERING & TECHNOLOGY

(Approved by AICTE, Govt. of Maharashtra & Affiliated to University of Mumbai*)
(Accredited Programmes by National Board of Accreditation, New Delhi**)

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Shyamnarayan Thakur Marg, Thakur Village,
Kandivali (East), Mumbai - 400 101.

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ISO 9001 : 2008 Certified

*Permanent Affiliated UG Programmes : • Computer Engineering • Electronics & Telecommunication Engineering • Information Technology (w.e.f. A.Y.2015-16 onwards)

**1st time Accredited UG Programmes : • Computer Engineering • Electronics & Telecommunication Engineering • Information Technology

**2nd time Accredited UG Programmes : • Computer Engineering • Electronics & Telecommunication Engineering • Information Technology • Electronics Engineering (3 years w.e.f. 01-07-2016)

TCET/FRM/IP-02/09

Revision: A

Semester Plan (Theory)

Semester: III

Course: EXTC

Subject: Digital System Design

Class: SE- B

Sr. No	Module No.	Lesson No.	Topics Planned (Technology to be used)	Teaching Aids Required	Planned /Completion Date	Resource Book Reference	Remarks
1	-	-	SOP	LCD Projector	10/07/17	-	
2	-	-	Lab-Orientation	LCD Projector	11/07/17	-	
3	-	-	OBE	LCD Projector	12/07/17	-	
4	1	1.1	Number Systems and Codes: Review of Number System, Binary Code	Chalk & Blackboard	13/07/17	R. P. Jain	
5	1	1.2	Octal Code, Hexadecimal Code and their conversions	Chalk & Blackboard	14/07/17	R. P. Jain	
6	1	2.1	Binary Coded Decimal, Gray Code	Chalk & Blackboard	17/07/17	R. P. Jain	
7	1	2.2	Binary Arithmetic	Chalk & Blackboard	18/07/17	R. P. Jain	

Sr. No	Module No.	Lesson No.	Topics Planned (Technology to be used)	Teaching Aids Required	Planned /Completion Date	Resource Book Reference	Remarks
8	2	2.3	Logic Gates and Combinational Logic Circuits: Analog and Digital signals and systems, Logic levels, Digital logic gates	Chalk & Blackboard	19/07/17	R. P. Jain	
9	2	2.4	Realization using NAND, NOR gates	Chalk & Blackboard	20/07/17	R. P. Jain	
10	2	2.5	Boolean Algebra, De Morgan's Theorem	Chalk & Blackboard	21/07/17	R. P. Jain	
11	2	3.1	SOP representation	Chalk & Blackboard	24/07/17	John F. Warkerly	
12	2	3.2	POS representation	Chalk & Blackboard	26/07/17	John F. Warkerly	
13	2	3.3	K-map introduction and examples of 2 and 3 variables	LCD Projector, Chalk & Blackboard	27/07/17	John F. Warkerly	
14	2	3.4	K-map up to four variables	LCD Projector, Chalk & Blackboard	28/07/17	John F. Warkerly	
15	2	4.1	Quine-McClusky method of minimization of logic expressions	LCD Projector, Chalk & Blackboard	31/08/17	John F. Warkerly	
16	2	4.2	Quine-McClusky numericals	LCD Projector, Chalk & Blackboard	02/08/17	John F. Warkerly	

Sr. No	Module No.	Lesson No.	Topics Planned (Technology to be used)	Teaching Aids Required	Planned /Completion Date	Resource Book Reference	Remarks
17	2	4.3	Arithmetic Circuits: Half adder, Full adder	Chalk & Blackboard	03/08/17	John F. Warkerly	
18	2	4.4	Half Subtractor, Full Subtractor	Chalk & Blackboard	04/08/17	John F. Warkerly	
19	2	5.1	Serial and Parallel Addition, Carry Look ahead adder	LCD Projector, Chalk & Blackboard	07/08/17	R. P. Jain	
20	2	5.2	BCD adder. Binary Multiplier,	LCD Projector	09/08/17	R. P. Jain	
21	2	5.3	Magnitude Comparator 1 bit & 2 bit	LCD Projector, Chalk & Blackboard	10/08/17	R. P. Jain	
22	2	5.4	Multiplexer and De-multiplexer: Multiplexer operations, Cascading of Multiplexer	Chalk & Blackboard	11/08/17	R. P. Jain	
23	2	6.1	Boolean Function implementation using multiplexer and basic gates, demultiplexer	LCD Projector, Chalk & Blackboard	14/08/17	R. P. Jain	
24	2	6.2	Encoder and Decoder	LCD Projector, Chalk & Blackboard	16/08/17	R. P. Jain	
25	2	6.3	TTL Logic families and their characteristics	LCD Projector, Chalk & Blackboard	18/08/17	Morris Mano / Michael D. Ciletti	

Sr. No	Module No.	Lesson No.	Topics Planned (Technology to be used)	Teaching Aids Required	Planned /Completion Date	Resource Book Reference	Remarks
26	2	7.1	CMOS Logic families and their characteristics	LCD Projector, Chalk & Blackboard	24/08/17	Morris Mano / Michael D. Ciletti	
27	4	8.1	Sequential Logic Circuits: Difference between combinational & sequential circuits, RS Flip flop	LCD Projector, Chalk & Blackboard	28/08/17	Morris Mano / Michael D. Ciletti	
28	4	8.2	JK and Master slave flip flops	LCD Projector, Chalk & Blackboard	30/08/17	Morris Mano / Michael D. Ciletti	
29	4	8.3	T & D flip flops, Level triggering & edge triggering of flip-flops	LCD Projector, Chalk & Blackboard	31/08/17	Morris Mano / Michael D. Ciletti	
30	4	8.4	Conversion of flip flops from one to another	LCD Projector, Chalk & Blackboard	01/09/17	Morris Mano / Michael D. Ciletti	
31	4	9.1	Registers: SISO, SIPO, PISO, PIPO, Universal shift registers	LCD Projector	04/09/17	Morris Mano / Michael D. Ciletti	
32	4	9.2	Counters: Asynchronous counter,	LCD Projector, Chalk & Blackboard	06/09/17	Morris Mano / Michael D. Ciletti	
33	4	9.3	Synchronous Counter, Up/Down counter	LCD Projector, Chalk & Blackboard	07/09/17	Morris Mano / Michael D. Ciletti	
34	4	9.4	MOD-N, BCD counter	LCD Projector, Chalk & Blackboard	08/09/17	Morris Mano / Michael D. Ciletti	

Sr. No	Module No.	Lesson No.	Topics Planned (Technology to be used)	Teaching Aids Required	Planned /Completion Date	Resource Book Reference	Remarks
35	4	10.1	Applications of Sequential Circuits: Frequency division, Ring Counter, Johnson Counter.	LCD Projector, Chalk & Blackboard	11/09/17	Thomas L. Floyd	
36	4	10.2	State machines, State transition diagram	LCD Projector	13/09/17	Thomas L. Floyd	
37	4	10.3	Design of Moore and Mealy circuits	LCD Projector, Chalk & Blackboard	14/09/17	Thomas L. Floyd	
38	4	10.4	Design of Serial Adder and vending Machine	LCD Projector	15/09/17	Thomas L. Floyd	
39	4	11.1	State Reduction Techniques: Row elimination and Implication table methods	LCD Projector, Chalk & Blackboard	18/09/17	Morris Mano / Michael D. Ciletti	
40	5	11.2	Programmable Logic Devices: Introduction : Programmable Logic Devices (PLD), Keyboard Encoder system design using PLD	LCD Projector, Chalk & Blackboard	20/09/17	Morris Mano / Michael D. Ciletti	
41	5	11.3	Programmable Logic Array (PLA), Programmable Array Logic(PAL)	LCD Projector	21/09/17	Morris Mano / Michael D. Ciletti	
42	6	11.4	VHSIC Hardware Description Language (VHDL): Data types, Structural modeling using VHDL	LCD Projector	22/09/17	J. Bhaskar	
43	6	12.1	Attributes, Data Flow model and behavioral modeling using VHDL	LCD Projector	25/09/17	J. Bhaskar	

Sr. No	Module No.	Lesson No.	Topics Planned (Technology to be used)	Teaching Aids Required	Planned /Completion Date	Resource Book Reference	Remarks
44	6	13.1	Implementation of Priority Encoder and combinational circuit using VHDL	LCD Projector	04/10/17	Volnei A. Pedroni	
45	6	13.2	Sequential circuits using VHDL	LCD Projector	05/10/17	Volnei A. Pedroni	
46.	6	13.3	Fibonacci Series Generator	LCD Projector	06/10/17	Volnei A. Pedroni	
47.	2	14.1	Different Types of Memory: Classification and Characteristics of memory, SRAM, DRAM	LCD Projector	09/10/17	Morris Mano / Michael D. Ciletti	
48.	2	14.2	ROM, PROM, EPROM and Flash memories	LCD Projector	11/10/17	Morris Mano / Michael D. Ciletti	
49.	-	14.3	University paper doubt solving	LCD Projector, Chalk & Blackboard	12/10/17		
Remark:: Course:		Syllabus Coverage:		Practice Session: 1. K-Map 2. Quine Mc-cluskey 3. Counter Design 4. State Machine Design		Beyond Syllabus: 1. K-map with 5 variables 2. 16 variable SOP expression design with 4:1 Mux	
No. of (lectures planned)/(lecture taken): (49)							

Text Books:

1. John F. Warkerly, "Digital Design Principles and Practices", Pearson Education, 4th Edition (2008).
2. R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill Education, Third Edition (2003).
3. J. Bhaskar, "VHDL Primer", PHI, Third Edition (2009).
4. Volnei A. Pedroni, "Digital Electronics and Design with VHDL" Morgan Kaufmann Publisher (2008)

Reference Books:

1. Morris Mano / Michael D. Ciletti, "Digital Design", Pearson Education, Fourth Edition (2008).
2. Thomas L. Floyd, "Digital Fundamentals", Pearson Prentice Hall, Eleventh Global Edition (2015).
3. Mandal, "Digital Electronics Principles and Applications", McGraw Hill Education, First Edition (2010).
4. Stephen Brown & Zvonko Vranesic, "Fundamentals of Digital Logic Design with VHDL", 2nd Edition, TMH (2009).
5. Ronald J. Tocci, Neal S. Widmer, "Digital Systems Principles and Applications", Eighth Edition, PHI (2003)
6. Donald P. Leach / Albert Paul Malvino /Gautam Saha, "Digital Principles and Applications", The McGraw Hill, 7th Edition (2011).

Digital Reference:

- Wikipedia
- Google
- Architecture of FPGAs and CPLDs: A Tutorial by Stephen Brown and Jonathan Rose
- <http://www.xilinx.com>

Sd/-

Payel Saha

Name & Signature of Faculty

Sd/-

Signature of HOD

Sd/-

Signature of Principal
/Dean (Academics)

Date:

Date:

Date:

Note:

1. Plan date and completion date should be in compliance
2. Courses are required to be taught with emphasis on resource book, course file, text books, reference books, digital references etc.
3. Planning is to be done for 15 weeks where 1st week will be AOP, 2nd -13th for effective teaching and 14th -15th week for effective university examination oriented teaching, mock practice session and semester consolidation.
4. According to university syllabus where lecture of 4 hrs/per week is mentioned minimum 55 hrs and in case of 3 lectures per week minimum 45 lectures are to be engaged are required to be engaged during the semester and therefore accordingly semester planning for delivery of theory lectures shall be planned.
5. In order to improve score in NBA, faculty members are also required to focus course teaching beyond university prescribed syllabus and measuring the outcomes w.r.t learning course and programme objectives.
6. Text books and reference books are available in syllabus. Here only additional references w.r.t. non – digital/ digital sources can be written (if applicable)
7. Technology to be used in class room during lecture shall be written below the topic planned within the bracket.